

## Laboratory Experiment #7: Simple Logic Circuits

### I. OBJECTIVES

The various operational modes of diodes and bipolar junction transistors will be investigated using simple diode logic (DL), diode-transistor logic (DTL), and transistor-transistor logic (TTL) gates. Confirm by computer simulations (SPICE).

### II. INTRODUCTION

Logic operations can be performed using any non-linear device that has at least two distinct regions of operation. Obvious choices for the electrical engineer are the semiconductor diode and the bipolar junction transistor. Particular voltage levels are assigned to logic levels 0 and 1. While many voltage level assignments are possible, one common assignment is:

$$\begin{aligned} \text{logic } 1 & \text{ ---- } \sim 5 \text{ V} \\ \text{logic } 0 & \text{ ---- } \sim 0 \text{ V.} \end{aligned}$$

It is important to note that noise, power source fluctuations, loading by other circuits, and other factors will cause the logic level voltages to vary over some range. Each logic gate type has its individual range of logic level voltage variation. Three logic types will be investigated: the diode logic (DL), diode-transistor logic (DTL), and transistor-transistor logic (TTL) gates.

Diode logic gates utilize the properties of a semiconductor diode in forward or reverse bias conditions. These gates have limited use due to the obvious logic level shift when gates are connected in series. They can, however, be useful for adding a gate or two to complex circuitry without adding integrated circuit chips. This type of logic circuit is rarely found in integrated form.

Diode-transistor logic gates use diodes in the input stage and a bipolar junction transistor as an output stage. The output BJT switches between its cut-off and saturation regions to create logic 1 and 0, respectively. DTL circuits are rarely found in integrated circuits today.

Transistor-transistor logic is commonly found in relatively low speed applications. TTL uses bipolar transistors in the input and output stages. The input diodes are replaced by a BJT with a multiple-emitter structure and switches between the various modes of BJT operation.

The logic level shift problem of DL gates is not present in DTL and TTL gates so that gates may be connected in series indefinitely. If a gate drives several similar gates in parallel problems may occur: the maximum number of gates that can be driven in parallel is identified as the "fan-out" of a gate. Various internal configurations of the internal circuitry of a gate can vary the fan-out of the gate.

### III. PROCEDURE

#### A. *Simulate the DL circuit of Figure 6-1.*

Simulate voltages equivalent to logic 1 and 0 to each of the inputs, measure the output voltage and determine the logic function of the gate. Notice that one of the output logic voltage levels does not exactly match the input logic voltage level. Change the input voltage levels to these measured output levels and repeat the determination of the logic function of the gate. Comment on any differences and compare to theory.

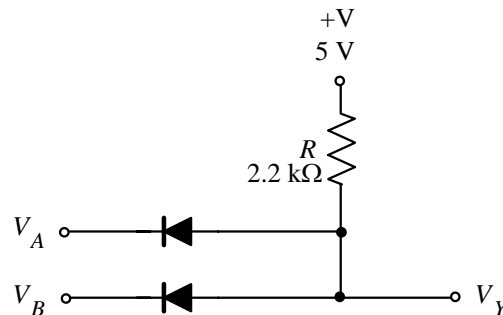


Figure 6-1. Diode Logic Circuit of Part A

#### B. *Connect the DL circuit of Figure 6-2.*

Repeat Section A. Notice that the opposite logic level voltage has changed and that the voltage difference between a logic 0 and logic 1 has been reduced. Estimate how many of these gates (a mixture of the two DL types) could be connected in series before a logic 1 and a logic 0 could be confused.

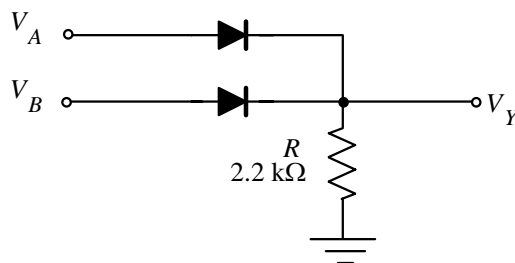


Figure 6-2 Diode Logic Circuit of Part B

#### C. *Simulate DTL the circuit of Figure 6-3a.*

Simulate voltages equivalent to logic 1 and 0 to each of the inputs, measure the output and determine the logic function of the gate. Attach one input to a logic level 1 and vary the voltage input to the other input between 0 V and 5 V. Plot the output voltage as a function of this input voltage. Comment on the difference seen with this gate as compared to the two DL gates.

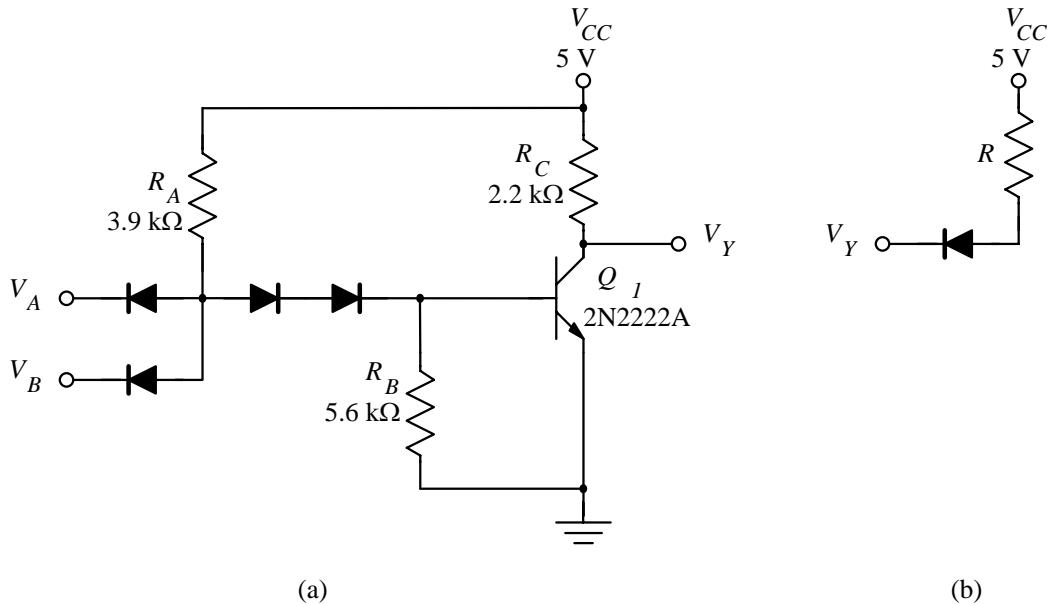


Figure 6-3. (a) DTL Gate  
(b) Simulated Load for Fan-Out Measurements

Attach a simulated load (Figure 6-3b.) to the output of this gate when both inputs are at logic 1. This simulated load models the input of several similar gates connected in parallel. Vary resistor  $R$  from 3.9 k $\Omega$  until the gate output level changes by at least 0.1 V.

Use SPICE to model this DTL gate. Simulate the experiment where one input is at 5V and the other varies from 0 V to 5 V. Plot the output voltage as a function of this varying input voltage. Monitor appropriate currents and/or voltages so that the state of each diode and transistor can be determined. On the output plot, identify the diode and transistor regions of operation. Compare simulation to experiment.

#### D. Simulate the circuit of Figure 6-4

Simulate voltages equivalent to logic 1 and 0 to each of the inputs, measure the output and determine the logic function of the gate. Attach one input to a logic level 1 and vary the voltage input to the other input between 0 V and 5 V. Plot the output voltage as a function of this input voltage. Comment on the difference seen with this gate as compared to DTL gates.

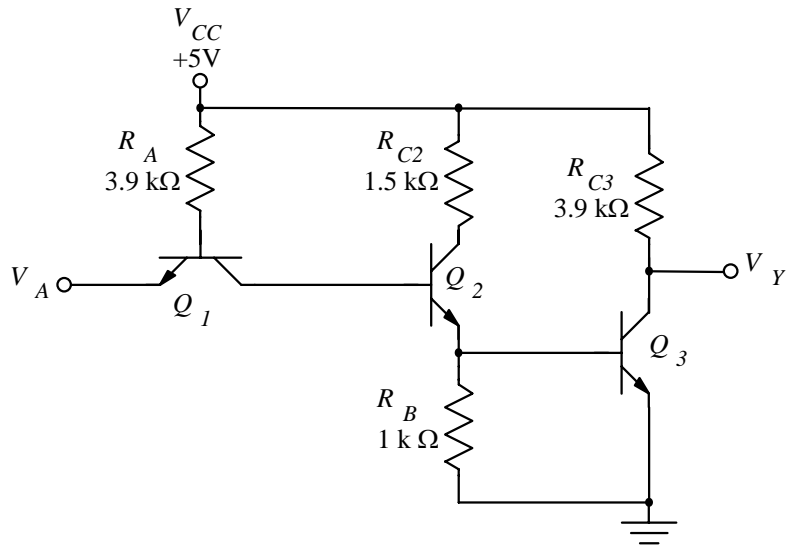


Figure 6-4. Single Input TTL Gate

Attach a simulated load (Figure 6-3b) to the output of this gate when both inputs are at logic 1. This simulated load models the input of several similar gates connected in parallel. Vary resistor  $R$  from  $3.9\text{ k}\Omega$  until the gate output level changes by at least  $0.1\text{ V}$ .

Simulate the experiment where one input is at  $5\text{ V}$  and the other varies from  $0\text{ V}$  to  $5\text{ V}$ . Plot the output voltage as a function of this varying input voltage. Monitor appropriate currents and/or voltages so that the state of each transistor can be determined. On the output plot, identify the transistor regions of operation.

*F. Comment on the results*