Laboratory Experiment #6: Biasing Bipolar Junction Transistors

I. OBJECTIVES

The common-emitter terminal characteristics of a Bipolar Junction Transistors (BJTs) will be determined experimentally using a commercial transistor curve tracer. The data will then be compared to equivalent models available in PSpice. A modified PSpice model will be developed that corresponds closely with the experimental data. Load-line analysis will be used to design the appropriate bias networks.

II. INTRODUCTION

A BJT is comprised basically of three doped semiconductor regions forming two p-n junctions connected back to back. The three semiconductor regions are identified as: the Base (B), the collector (C), and the emitter (E). The labeling codes "npn" and "pnp" identify the doping the three semiconductor regions that make up a BJT: npn implies n-type doping of the collector and emitter and p-type doping of the base; pnp implies the inverse. While the collector and emitter are always of the same doping type, the doping concentrations may be different in those two regions.

The operation of a BJT depends on both electron and hole conduction. Depending on the bias of each of the two p-n junctions, the BJT operates in one of four distinct regions as shown in Figure 5-1.

In linear applications, BJT circuits must be designed so that the transistor operates in the forward-active region. In order to insure operation in the forward-active region, the transistor is biased at a quiescent operating point, commonly called the Q-point, based on the DC conditions.
of the BJT. The quiescent point is determined by the transistor input and output characteristics and the applied currents and voltages. The quiescent point is defined by the BJT DC quantities $V_{BE}$, $I_B$, $V_{CE}$, and $I_C$. These points may be determined through the use of load-line analysis and design methods.

The biasing configurations that are to be investigated are the fixed-bias and self-bias circuits shown in Figures 6-2a and 6-2b, respectively.

![Figure 6-2. (a) Fixed-Bias Circuit Configuration (b) Self-Bias Circuit Configuration](image)

For the Q-point in the forward active region, $V_{BE} = 0.7V$. In order design and analyze a biased circuit, we require the BJT $\beta_F$ for finding the base current from the collector current (or vice-versa).

For the Fixed-Bias circuit shown in Figure 6-2a, the base-emitter KVL analysis yields

$$0 = V_{CC} - I_B R_B - V_{BE}$$

and the collector-emitter KVL analysis yields

$$0 = V_{CC} - I_C R_C - V_{CE}$$

Use the relationship $I_C = \beta_F I_B$ to solve for appropriate $R_B$ and $R_C$ values given $V_{CC}$, and Q-points.

The Self-Bias circuit in Figure 6-2b requires conversion of the subcircuit connected to the base of the BJT to be converted to the Thevenin equivalent circuit for ease of design and analysis. Figure 6-3 shows the transformation of the self-bias circuit using Thevenin equivalents.
Figure 6-3. Self-Bias Circuit Design and Analysis: (a) Self-Bias Circuit, (b) Re-Arranged Circuit, and (c) Thevenin Equivalent Circuit

So the Base-Emitter KVL equation for the Thevenin Equivalent circuit is:

\[
0 = \frac{V_{CC}R_{B2}}{R_{B1} + R_{B2}} - I_B \left(R_{B1} \, || \, R_{B2}\right) - V_{BE} + I_E R_E
\]

and the Collector-Emitter KVL equation is:

\[
0 = V_{CC} - I_C R_C - V_{CE} + I_E R_E
\]

Recall that \(I_E = - (\beta_F + 1) I_B\) and \(I_E = -I_C \left(\frac{\beta_F + 1}{\beta_F}\right)\).

Note also that \(\frac{V_{CC}R_{B2}}{R_{B1} + R_{B2}} = \frac{V_{CC} \left(R_{B1} \, || \, R_{B2}\right)}{R_{B1}}\). This equation may simplify design when analyzing the Base-Emitter KVL loop.

III. PROCEDURE

A. Common-Emmitter Output Transfer Curve

Examine the 2N222A BJT and, with the help of Figure 4-3, identify the base, emitter, and collector terminals. Using a commercial curve tracer, measure and plot the common-emitter configuration characteristics.
Find $V_{BE}$, $V_{CE}$, $I_C$, and $I_B$ at the point where the collector-emitter voltage is 5 V and the collector current is 2.5 mA. Use the $\beta_F$ determined by the LabVIEW curve tracer program to find $I_B$ from $I_C$.

B. Common-Emitter Transfer Curves Using PSpice BIPOLAR.LIB Models
For those BJTs that have a PSpice model (in BIPOLAR.LIB in the PSpice subdirectory) model the experiments of sections A and B and obtain the data curves. Compare these modeled results to experimental results and comment on similarities and/or differences.

C. Common-Emitter Transfer Curves Using Customized PSpice Models
Create PSpice BJT models based on the parameters found from the measured input and output characteristics and obtain the V-I curves. Compare with experimental data and models found in BIPOLAR.LIB.

D. Load-Line Analysis and Design
Design a bias circuit using load-line analysis for $V_{CE} = 5$ V and $I_C = 2.5$ mA for the two bias networks shown in Figure 4-2. The characteristic curves shall be created from your customized PSpice model of the BJTs. Let $V_{CC} = 15$ V.

Circuit 6-2a
Let $R_C = 4$ k$\Omega \approx 3.9$ k$\Omega$ (10% resistor). Find $R_B$ given your measured BJT $\beta_F$. Show your $R_B$ calculation. The value of $R_B$ should be in or around 1 M$\Omega$.

Circuit 6-2b
Let $R_E = 1.2$ k$\Omega \approx 1.8$ k$\Omega$, $R_C = 2.8$ k$\Omega \approx 2.7$ k$\Omega$, and $R_{B1} = 33$ k$\Omega$ (10% resistors). The value of $R_{B2}$ is in the order of 10 k$\Omega$. Show your $R_{B2}$ calculation.

E. Verification
Verify your experimental data with both the original load-line analysis and PSpice simulations.